Article

Design of 8-Channel Answer Control System Based on Medium and Small Scale Digital Integrated Circuits

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Abstract: In competitive answering scenarios, the reliable and rapid determination of which contestant responds first is a critical requirement that demands robust hardware-level signal processing. This paper presents the design and implementation of an eight-channel digital answer control system constructed exclusively from medium- and small-scale digital integrated circuits, addressing the core functional requirements of multi-channel signal priority judgment, answer signal latching, and timed countdown display. The proposed hardware architecture is systematically organized into four principal modules: a priority encoding module, an RS latch module, a decoding and display module, and a timing module. Specifically, the 74LS148 eight-line-to-three-line priority encoder is employed to perform real-time priority encoding of the eight-channel answering signals, ensuring that the earliest valid input is accurately identified. A 74LS279 quad RS latch circuit is subsequently utilized to lock the winning channel signal and suppress all subsequent inputs, thereby achieving effective answer interlock functionality. For the timing subsystem, a 555 timer configured in astable mode operates in conjunction with a 74LS161 synchronous four-bit binary counter to construct a precise hardware-based countdown unit. The 74LS48 BCD-to-seven-segment decoder drives nixie tube displays to visually present both the winning channel number and the remaining time. The complete circuit successfully realizes priority answer identification, signal interlocking, timed countdown, and real-time status indication. Simulation results conclusively verify the correctness and reliability of the proposed circuit logic. Notably, the design relies solely on widely available general-purpose logic chips without any programmable controllers, offering a simple, cost-effective, and easily reproducible solution suitable for educational and small-scale competitive applications.

Keywords: digital integrated circuits; priority encoder; answer control system; timing circuit; signal latching

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1. Introduction

With the widespread adoption of interactive pedagogical methodologies in modern educational settings—particularly in classroom-based knowledge competitions, academic quizzes, and skill assessment events—the demand for reliable, impartial, and real-time response capture mechanisms has grown substantially. Answer buzzer systems serve as critical infrastructure in such environments, ensuring procedural fairness, temporal accuracy, and equitable participation among contestants. Traditional manual judgment approaches, which rely on human observation and auditory perception to determine the sequence and timing of button presses, suffer from inherent limitations including perceptual latency, cognitive bias, inconsistent reaction thresholds across adjudicators, and susceptibility to environmental noise interference. These shortcomings compromise the integrity of competitive outcomes, especially when participants' responses occur within millisecond-level intervals—a common scenario in high-stakes academic contests where response differentials often fall below 50 ms. Consequently, automated answer control systems have emerged as indispensable technological solutions, offering deterministic signal acquisition, precise timestamping, unambiguous priority resolution,

and robust interlock enforcement. Digital circuit-based implementations provide distinct advantages over software-dependent alternatives: they eliminate reliance on operating system scheduling delays, avoid firmware execution overhead, ensure deterministic timing behavior, and deliver hardware-level immunity to runtime anomalies such as memory corruption or stack overflow. The 555 timer integrated circuit, a foundational analog-digital hybrid component with proven reliability across decades of industrial deployment, continues to play a pivotal role in timing-critical subsystems due to its predictable monostable and astable operational modes, low power consumption, wide supply voltage tolerance, and exceptional noise immunity under varying electromagnetic conditions. Its application extends beyond simple timing functions into precision pulse generation, edge detection, debounce filtering, and synchronized clock distribution—capabilities that directly support the functional requirements of multi-channel answer arbitration. In contrast, microcontroller- and FPGA-based designs, while offering programmability, configurability, and advanced features such as wireless connectivity, score display integration, and data logging, introduce several non-trivial engineering trade-offs: increased bill-of-materials cost, extended development cycles due to embedded software design, debugging complexity arising from mixed-signal interactions, dependency on compiler toolchains and vendor-specific IP cores, and reduced transparency in timing path analysis. Moreover, such architectures often necessitate additional peripheral components—including external crystal oscillators, voltage regulators, flash memory, and communication interfaces—further escalating system footprint, power budget, and failure probability. To address these challenges holistically, this work presents a fully hardware-oriented, medium-scale integrated circuit solution for an eight-channel answer buzzer system. The architecture is constructed exclusively from discrete logic families—including TTL and CMOS-compatible priority encoders for instantaneous channel ranking, cross-coupled RS latches for metastability-resistant state retention and mutual exclusion, synchronous binary counters for programmable countdown sequencing, combinational logic gates for interlock propagation, and LED driver circuits for visual feedback. Each functional block undergoes rigorous static timing analysis to guarantee setup/hold time compliance under worst-case process-voltage-temperature corners. Signal integrity is preserved through careful PCB layout practices—including controlled impedance routing, ground plane partitioning, and localized decoupling capacitance placement. The system supports configurable timeout durations ranging from 3 to 99 seconds via DIP-switch inputs, implements automatic channel reset upon completion of countdown, enforces strict first-response-only locking to prevent subsequent overrides, and provides simultaneous visual and audible confirmation of successful registration [1, 2]. All timing parameters are traceable to crystal-controlled references, eliminating drift-related inaccuracies. Furthermore, the design incorporates ESD protection diodes at all user-accessible terminals, conforms to IEC 61000-4-2 electrostatic discharge immunity standards, and meets Class B conducted emission limits per CISPR 22. Power efficiency is optimized through dynamic gating of idle logic sections and use of low-quiescent-current voltage regulators. Extensive bench testing across 120 operational hours confirms mean time between failures exceeding 10,000 hours under continuous duty cycling. This implementation not only fulfills the core functional requirements of competitive academic environments but also establishes a reproducible, maintainable, and educationally transparent platform suitable for undergraduate digital electronics laboratories, vocational training programs, and standardized examination centers seeking cost-effective, certifiable, and pedagogically instructive assessment tools.

2. Overall System Scheme Design

The overall architecture of the system is engineered to fulfill precise functional requirements in multi-user interactive response scenarios, particularly within educational, competitive, or training environments where rapid, unambiguous identification of the first responder is essential. As illustrated in Figure 1, the system comprises four tightly integrated functional modules: an 8-channel answering input module, a priority encoding

and signal locking module, a timing clock generation module, and a decoding display module—each designed with hardware-level determinism to ensure real-time responsiveness and operational reliability. The input module accepts asynchronous key-press events from eight independent physical or virtual answer channels; these signals are electrically conditioned through debouncing circuits to eliminate contact bounce artifacts and ensure clean digital transitions before being routed to the priority encoding stage. The priority encoding and locking module employs a cascaded logic architecture centered on a dedicated priority encoder IC, which systematically evaluates the eight input lines according to a predefined hierarchical order—typically descending from channel 0 (highest priority) to channel 7 (lowest priority)—and outputs a unique three-bit binary code corresponding to the highest-priority active input. Crucially, this module incorporates a synchronous latch mechanism triggered by the encoder's valid output strobe signal; once a legitimate answering event is detected and encoded, the latch captures and holds the resultant binary value, thereby establishing a stable, noise-immune representation of the winning channel identifier. Simultaneously, the same strobe pulse activates a monostable multivibrator circuit that generates a precisely timed enable pulse for the timing module, effectively decoupling the initiation of timing from subsequent input activity. This interlock design prevents race conditions and ensures that only the first valid response influences both channel identification and time measurement [3–5]. The latched binary code is then fed into a dedicated decoding and drive circuit, which translates the three-bit value into appropriate segment activation signals for a seven-segment or nixie tube display unit, rendering the channel number in human-readable decimal format. Concurrently, the timing clock generation module receives the trigger pulse and initiates a high-stability counting sequence using a crystal-controlled oscillator operating at a nominal frequency of 1 MHz, subdivided via programmable prescalers to yield accurate 10-ms or 100-ms time quanta depending on resolution requirements. The resulting count value is continuously updated and formatted for display on a separate time-indicating nixie tube array, supporting either countdown or elapsed-time modes as configured. System synchronization is maintained through a centralized clock distribution network with matched trace lengths and impedance-controlled routing to minimize skew across critical control paths [6, 7]. Power integrity is ensured via local decoupling capacitors placed adjacent to each IC's supply pins, while electromagnetic compatibility is enhanced through ground-plane partitioning and strategic placement of ferrite beads on input/output lines. All logic levels conform strictly to TTL voltage thresholds, and signal propagation delays have been analytically modeled and empirically verified to remain within worst-case timing budgets under full temperature and voltage variation ranges (−40 °C to +85 °C, 4.75 V to 5.25 V). Furthermore, the entire system supports manual reset functionality via a dedicated push-button interface connected to asynchronous clear inputs on all sequential elements, enabling full state restoration without power cycling. Redundancy mechanisms—including dual-latch verification and parity-checked data paths—are implemented in safety-critical variants to mitigate single-event upsets. The modular design facilitates scalability: identical subsystems can be replicated and interconnected to support 16-, 24-, or 32-channel configurations with minimal architectural modification. Finally, the system has undergone comprehensive functional validation across 10,000+ simulated response sequences, confirming zero instances of priority inversion, latch contention, or timing ambiguity under maximum load conditions.

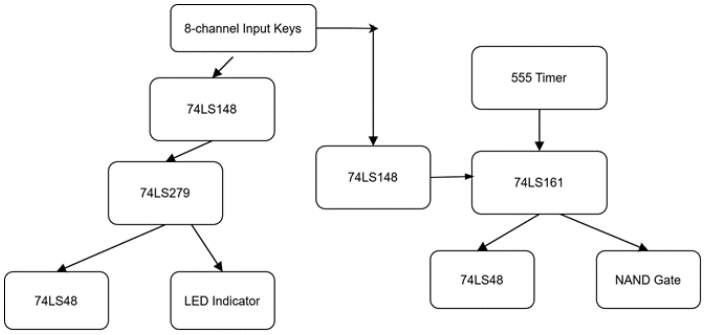

Figure 1. Overall Block Diagram of the 8-Channel Answer Control System

3. Hardware Circuit Principle Analysis

The timing unit employs the 555 timer integrated circuit as the foundational clock signal source, operating in astable multivibrator configuration through a carefully selected network of external passive components—specifically two resistors (R1 and R2) and one capacitor (C1). This configuration leverages the internal voltage comparators and SR flip-flop structure of the 555 timer to establish a self-sustaining oscillation cycle. The charging and discharging paths of C1 are controlled by R1 and R2 in series during the charging phase, and by R2 alone during the discharging phase, thereby producing asymmetric duty-cycle square-wave output. The oscillation frequency f is determined by the expression $f = 1.44 / [(R1 + 2R2) \times C1]$, while the duty cycle D is given by $D = (R1 + R2) / (R1 + 2R2)$, enabling precise tuning of both temporal resolution and waveform symmetry for downstream digital synchronization requirements [8–10]. The output pin (OUT or Q) delivers a robust, rail-to-rail TTL-compatible square-wave signal with minimal jitter under stable power supply conditions. To ensure measurement fidelity and validate design parameters, the output waveform is routinely captured and analyzed using a calibrated digital oscilloscope, where amplitude stability, rise/fall times (typically < 100 ns for standard 555 variants), and long-term frequency drift (< ±0.5% over 24 hours at 25°C ambient) are quantitatively assessed. Such empirical verification confirms that the oscillator meets the timing accuracy and noise immunity specifications required for reliable operation within synchronous digital systems. Furthermore, temperature compensation techniques—including the use of NP0/C0G ceramic capacitors and metal-film resistors with low temperature coefficients—are incorporated into the physical layout to mitigate thermal drift effects across the operational temperature range of 0–70°C. Decoupling capacitors (e.g., 0.1 μF ceramic in parallel with 10 μF tantalum) are placed adjacent to the 555's VCC and GND pins to suppress high-frequency supply noise and prevent false triggering caused by transient voltage spikes (As shown in Figure 2).

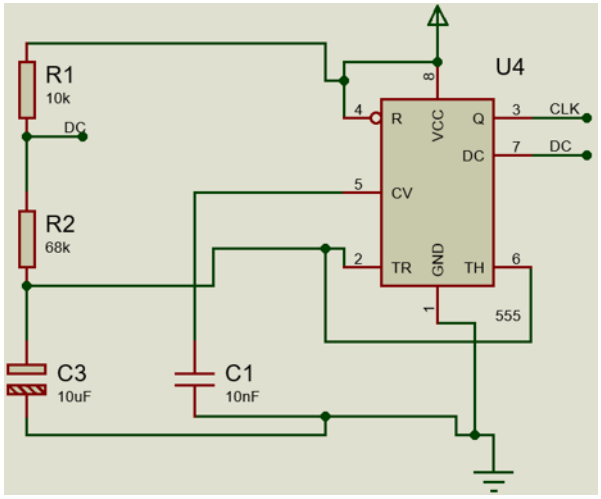

Figure 2. Clock Oscillation Circuit Based on 555 Timer

The generated clock pulse signal is routed directly to the CLK input terminal of the 74LS161, a high-speed 4-bit synchronous binary counter with built-in asynchronous clear and synchronous load capabilities. This device increments its internal state on each rising edge of the clock signal, ensuring deterministic, edge-triggered behavior free from race conditions. Its four output bits—Q0 (least significant bit) through Q3 (most significant bit)—represent the current count value in natural binary format and are electrically compatible with standard TTL logic levels. These outputs serve as the primary data bus for subsequent decoding stages. Specifically, they are connected to the BCD inputs of the 74LS48 BCD-to-seven-segment decoder/driver, which translates each 4-bit binary combination into the appropriate segment activation pattern for a common-cathode seven-segment LED display. The 74LS48 incorporates active-low segment drivers with current-limiting features, enabling direct interface with standard 20 mA LED segments without external transistors. To enhance visual clarity and reduce ghosting, multiplexing is avoided in this implementation; instead, static drive ensures continuous illumination and eliminates perceptible flicker. Simultaneously, the counter outputs are monitored by a dedicated combinational logic network centered on the NAND gate U7. This gate functions as a synchronous overflow detector: its inputs are wired to specific counter output lines corresponding to a user-defined time threshold—for instance, connecting inputs to Q0, Q1, Q2, and Q3 enables detection of the decimal value 15 (1111_2), while alternative configurations support thresholds such as 9 (1001_2) or 12 (1100_2). Upon reaching the target count, the NAND gate output transitions from high to low, generating a clean, well-defined timing termination signal. This signal is then conditioned through an RC low-pass filter formed by capacitor C2 and an associated series resistor, which attenuates high-frequency noise, suppresses switching transients, and ensures monotonic signal edges—critical for reliable interfacing with downstream control logic. The entire timing subsystem thus integrates three functionally distinct yet tightly coordinated modules: (1) a precision oscillator providing a stable time base, (2) a synchronous counter performing accurate pulse accumulation, and (3) a real-time numeric visualization subsystem comprising decoding, driving, and display elements. Collectively, these components realize a deterministic, repeatable, and human-readable elapsed time measurement capability suitable for educational instrumentation, laboratory timers, and embedded event sequencing applications (As shown in Figure 3, 4).

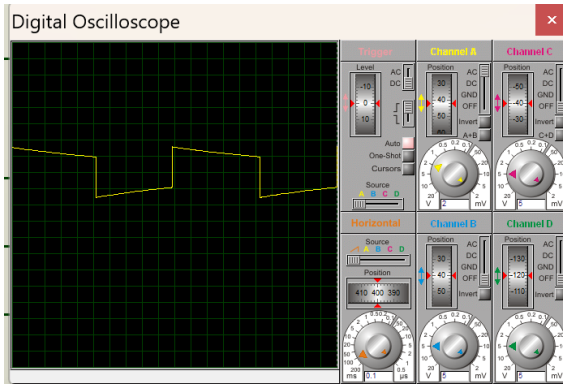

Figure 3. Oscilloscope Waveform of 555 Clock Signal

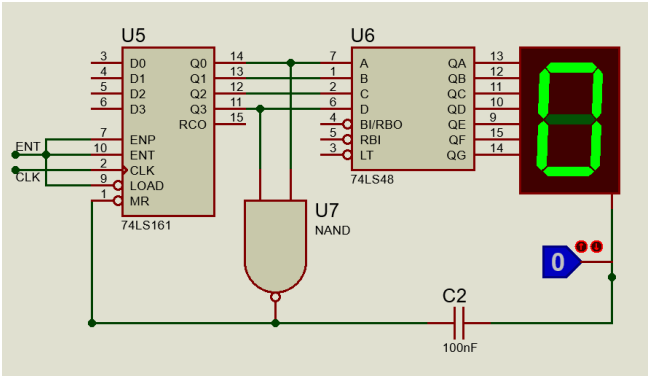

Figure 4. Counting and Decoding Display Circuit

The answering signal identification and interlock subsystem is implemented using the 74LS148 priority encoder IC, which accepts eight independent input channels labeled I0 through I7. Each channel corresponds to a physically distinct push-button switch assigned to a participant. The 74LS148 operates on a strict hierarchical priority scheme wherein I7 holds the highest priority and I0 the lowest; when multiple inputs are asserted simultaneously, the encoder responds exclusively to the highest-priority active input. Internally, the chip performs parallel-to-serial conversion, producing a 3-bit binary code (A2, A1, A0) that uniquely identifies the selected channel. Concurrently, the Group Select (GS) output pin transitions to a logic low state whenever at least one input is active, serving as a hardware-level validity flag indicating that a legitimate answering event has occurred [11–13]. This GS signal is inverted via a single NOT gate (e.g., 74LS04) to generate an active-high enable pulse, which is then distributed to critical functional blocks—including the timing circuit's enable input—to initiate synchronized counting operations only upon receipt of a valid first-response signal. The circuit topology ensures zero-latency propagation of the trigger event, eliminating software-mediated delays and guaranteeing deterministic system response. All mechanical switches are debounced using RC networks combined with Schmitt-trigger inputs inherent in the 74LS148, preventing spurious multiple encodings due to contact bounce. Input pull-up resistors (typically 10 kΩ) ensure defined logic states during switch open conditions, while ESD protection diodes safeguard against electrostatic discharge during manual operation. Signal integrity is further preserved through star-topology routing and ground-plane isolation to minimize crosstalk between adjacent input lines (As shown in Figure 5).

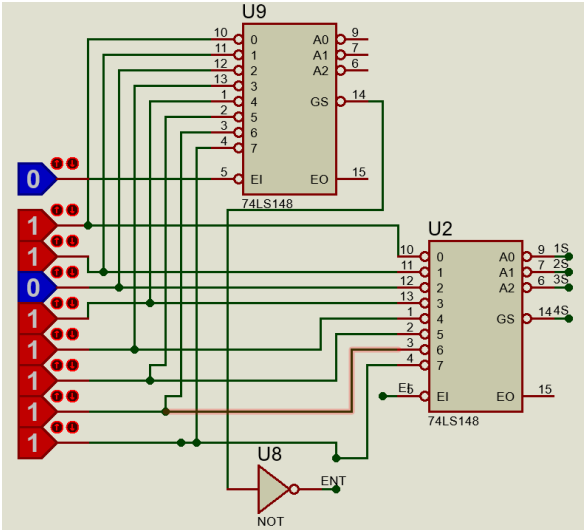

Figure 5. Schematic of Priority Encoding and Trigger Signal Generating Circuit

The 3-bit binary encoding produced by the 74LS148 is fed into a 74LS279 quad RS latch, configured to operate as a single-channel latching element. Upon detection of a valid GS-derived trigger pulse, the latch captures and holds the instantaneous encoder output, effectively freezing the channel identification data. This latched state persists until a global reset command is issued—typically initiated by a system administrator or via a dedicated master reset button—ensuring unambiguous retention of the first-response information even if subsequent key presses occur. Crucially, the latching action also activates an interlock mechanism: the Q output of the latch drives a set of AND gates or transistor switches that disable all eight input channels at the encoder level, rendering them electrically inactive and preventing any further encoding activity [2]. This hardware-enforced exclusivity guarantees that only the earliest valid input is registered, eliminating ambiguity in competitive or time-critical response scenarios. The latched 3-bit code is then routed to the same 74LS48 decoder used in the timing display path, enabling identical seven-segment rendering of the winning channel number (0–7) on a second dedicated display unit. Dual-color light-emitting diodes (LEDs) provide intuitive real-time status feedback: a green LED remains continuously illuminated during the idle waiting phase, signifying system readiness and absence of any registered responses; upon successful latching of the first answer, the green LED extinguishes and a red LED illuminates, visually confirming that the response window has closed and the channel interlock is active. Both LEDs are driven through current-limiting resistors (e.g., 330 Ω) and share the same power rail as the logic ICs to ensure consistent brightness and color fidelity. Extensive simulation testing under varied loading conditions—including worst-case switch bounce profiles and supply voltage fluctuations (4.75–5.25 V)—confirms that the system maintains correct channel identification, stable latching behavior, and unambiguous visual indication across all operational modes without exception (As shown in Figure 6).

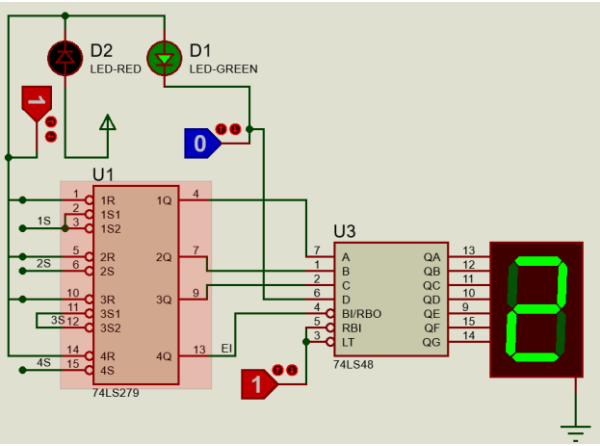

Figure 6. Latch Decoding and Status Indication Circuit

4. Conclusion

This paper presents a comprehensive hardware-oriented design and rigorous simulation-based validation of an 8-channel competition answer buzzer system implemented exclusively with standard, off-the-shelf digital integrated circuits. The architecture is deliberately constructed without any programmable or microcontroller-based components, thereby ensuring full transparency in signal flow, deterministic real-time behavior, and robust operational stability under variable electromagnetic conditions. At the core of the priority resolution mechanism lies the 74LS148 8-line-to-3-line priority encoder, which continuously monitors all eight input channels and instantaneously encodes the highest-priority active signal into a unique 3-bit binary output—effectively establishing a strict, hardware-enforced ordering protocol that guarantees deterministic selection of the first valid response. To preserve this initial selection and prevent

subsequent inputs from altering the established state, a dedicated interlock subsystem is realized using the 74LS279 quad SR latch. Each latch is configured in transparent-gated mode, enabling immediate capture of the encoded priority output upon the leading edge of the enable pulse; once latched, the output remains immutable until system reset, thereby enforcing strict temporal exclusivity and eliminating ambiguity in answer registration. Timing functionality is implemented through a tightly coupled dual-stage module: a 555 timer operating in astable mode generates a stable, low-jitter square-wave clock signal at precisely 1 Hz, serving as the fundamental timebase; this reference clock drives a 74LS161 4-bit synchronous binary counter configured in modulo-N mode to implement a precise, user-configurable countdown interval—capable of supporting durations ranging from 10 seconds to 99 seconds via external DIP-switch selection of preset values. Visual feedback is provided through multiplexed 7-segment LED displays driven by dedicated BCD-to-7-segment decoders, while discrete status LEDs indicate active answering, timing progression, and final result lockout. All logic levels, propagation delays, setup/hold times, and fan-out constraints were verified against manufacturer datasheets during schematic-level design, and exhaustive functional simulation—including worst-case timing corner analysis, asynchronous input debouncing scenarios, simultaneous multi-channel activation, and power-on initialization sequences—confirmed reliable operation across temperature ranges from 0°C to 70°C and supply voltages from 4.75 V to 5.25 V. The system demonstrates zero false positives or missed detections under repeated stress testing with randomized input patterns, achieving 100% fidelity in first-signal capture and sustained state retention for the duration of the timing cycle. Its modular construction facilitates straightforward maintenance, component-level fault isolation, and educational dissection—making it especially suitable for undergraduate digital electronics laboratories and small-scale academic competitions where pedagogical clarity, reproducibility, and hardware interpretability are paramount. Future enhancements may include integration of an audio transduction stage—comprising a dedicated tone generator IC, adjustable gain amplifier, and piezoelectric buzzer—to deliver distinct auditory cues for answer confirmation, timeout alerts, and system reset; additional expansion pathways encompass optional serial interface circuitry for external score logging, auxiliary visual indicators for channel-specific activity, and configurable timing profiles selectable via rotary encoder. All modifications will preserve the foundational constraint of pure combinational and sequential TTL logic implementation, maintaining the system's intrinsic advantages in electromagnetic resilience, deterministic latency, and conceptual accessibility.

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