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# Influence of Surface Morphology and Micro-Defects on the Electrical Performance and Implied Mechanical Reliability of Fine-Pitch Copper Bonding Wires

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**Abstract:** With the continuous miniaturization of semiconductor devices, copper (Cu) has largely replaced gold (Au) as the primary material for wire bonding due to its lower cost and superior electrical properties. However, the long-term reliability of copper wire interconnects is highly sensitive to material quality, particularly surface integrity. This study investigates the influence of surface morphology and manufacturing-induced micro-defects on the performance of fine-pitch palladium-coated copper (PCC) bonding wires. We employed Scanning Electron Microscopy (SEM) to perform a detailed morphological characterization, revealing the presence of longitudinal striations, pits, and critical transverse micro-cracks on the wire surface, which are artifacts of the wire drawing process. To quantitatively characterize the surface topography, Atomic Force Microscopy (AFM) was utilized, which provided high-resolution topographical data and quantified the significant nanoscale roughness of the defect-rich areas. Furthermore, the electrical properties were assessed using a four-point probe method. The results indicate that wires with pronounced surface defects exhibit a measurable increase in electrical resistivity. This is attributed to a combination of a reduced effective conductive cross-section and enhanced electron scattering at the roughened, defective surfaces. The observed micro-cracks are also discussed as potent stress concentration sites that could severely compromise the mechanical reliability and fatigue life of the interconnects. This work underscores the critical importance of controlling surface quality during the manufacturing of copper bonding wires to ensure the performance and long-term reliability of modern microelectronic packages.

**Keywords:** copper bonding wire; surface morphology; micro-defects; electrical resistivity; Atomic Force Microscopy (AFM); reliability; semiconductor packaging

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## 1. Introduction

The relentless pursuit of Moore's Law has driven the semiconductor industry towards ever-increasing integration densities, higher performance, and lower costs. This trend has placed immense pressure on all aspects of integrated circuit (IC) manufacturing, including the critical final stage of packaging and assembly [1]. IC packaging serves to protect the delicate silicon die, provide electrical connections to the external circuitry, and facilitate thermal dissipation. Among the various interconnection technologies, wire bonding remains the most dominant and cost-effective method for creating electrical pathways from the IC chip pads to the lead frame or substrate. For decades, gold (Au) was the undisputed material of choice for bonding wires, owing to its excellent electrical conductivity, superior corrosion resistance, and remarkable ductility, which facilitates the formation of reliable bonds.

However, the volatile and perpetually high price of gold has been a significant driver for the industry to seek alternative materials. In this context, copper (Cu) has emerged as

the most viable successor [2]. Copper offers several compelling advantages over gold, including higher electrical and thermal conductivity, slower intermetallic compound formation, and significantly lower material cost. The transition from gold to copper, initiated in the early 2000s, has now become mainstream, especially for fine-pitch applications where wire diameters are pushed down to 20 μm or less.

Despite its benefits, the adoption of copper wire is not without its challenges. Copper is inherently harder than gold, which can lead to pad damage during the ultrasonic bonding process. More critically, copper is highly susceptible to oxidation when exposed to air, which can impede bond ability and degrade long-term reliability. To mitigate this, commercial copper wires are often coated with a thin, inert layer of palladium (Pd), creating what is known as palladium-coated copper (PCC) wire. This coating effectively prevents oxidation and enhances the bonding performance.

Beyond these well-documented challenges, a more subtle yet crucial factor governing the performance and reliability of copper bonding wires is their surface quality. The wire manufacturing process, primarily involving multiple stages of extrusion and die drawing, is an aggressive mechanical deformation process. While it effectively reduces the wire to its final fine diameter, it inevitably introduces a variety of surface and subsurface imperfections. These can range from relatively benign, directionally aligned drawing marks (striations) to more severe defects such as deep scratches, embedded particles, and microcracks.

The surface of the bonding wire is the primary interface for both the bonding process and its interaction with the operating environment. A rough or defective surface can negatively impact the formation of the free-air ball (FAB) at the capillary tip, affect the loop shape, and compromise the integrity of the stitch bond on the lead frame. More importantly, over the lifetime of the device, these surface defects can act as initiation sites for failure mechanisms. Therefore, the seemingly cosmetic aspect of surface finish is, in fact, intrinsically linked to the fundamental mechanical and electrical reliability of the entire packaged device. This study is motivated by the need for a deeper understanding of this link.

## 2. Research Hypotheses

Based on the established challenges in copper wire manufacturing and the fundamental principles of materials science, this study is built upon a series of interconnected hypotheses regarding the surface integrity of commercial fine-pitch copper wires and its subsequent impact on performance [3,4]. We first hypothesize that the aggressive mechanical drawing process, inherent to wire manufacturing, inevitably imparts a distinct and non-ideal topography onto the wire surface. It is anticipated that high-resolution imaging via Scanning Electron Microscopy (SEM) provided by Wellrun Technology Co., Ltd. will reveal not only the ubiquitous, directionally aligned striations that are a standard byproduct of the process, but also more severe, localized defects such as transverse micro-cracks, pits or embedded particles. These flaws represent significant deviations from a perfectly cylindrical conductor.

Building on this initial premise, we further hypothesize that the surface topography observed qualitatively by SEM can be quantitatively characterized at the nanoscale. Specifically, it is proposed that the defect-rich areas, particularly those dominated by drawing striations, possess a significant degree of surface roughness [5]. We expect that Atomic Force Microscopy (AFM) can provide high-resolution, three-dimensional maps of this landscape, yielding quantitative roughness parameters, such as the arithmetic average roughness (Ra), which will confirm the substantial nanoscale asperity of the surface. This quantitative step is crucial for moving beyond simple observation to understanding the physical dimensions of the surface imperfections.

The central hypothesis of this investigation posits that these well-characterized morphological and topographical features will have a tangible and detrimental effect on the

wire's key functional properties. We propose that the presence of both severe micro-cracks and generalized high surface roughness will culminate in a measurable increase in the wire's electrical resistivity. This anticipated degradation in electrical performance is attributed to a dual mechanism: firstly, the geometric constriction of the current path caused by non-conductive micro-cracks, which reduces the effective current-carrying cross-section; and secondly, an increase in electron scattering events at the rough conductor surface, a phenomenon known to impede electron mobility and increase resistance, especially in fine-diameter wires where surface-to-volume ratios are high. The validation of this chain of hypotheses would therefore establish a direct link from manufacturing-induced surface defects to a quantifiable degradation in electrical performance.

## 3. Research Design

To systematically test the proposed hypotheses, a multi-faceted characterization approach was designed, focusing on a synergistic combination of morphological, topographical, and electrical analyses [6]. The material under investigation was a commercially available, high-performance palladium-coated copper (PCC) bonding wire with a nominal diameter of 20 μm. According to the manufacturer's specifications, the core material was 4N-grade (99.99%) pure copper, which was coated with a thin layer of palladium (estimated thickness ~30-50 nm) to prevent oxidation and enhance bondability. Samples of the wire were carefully cut from the spool for analysis, ensuring that no additional mechanical damage was introduced prior to characterization.

The investigation began with a detailed examination of the wire's surface morphology using a Scanning Electron Microscope (SEM, the F-series Scanning Electron Microscope of Wellrun Technology Co., Ltd.). Wire segments were mounted on an aluminum SEM stub with conductive carbon tape. Imaging was performed with a secondary electron (SE) detector under an accelerating voltage of 15.0 kV and at a working distance of approximately 10 mm to obtain high-resolution images across a range of magnifications [7]. This initial step was foundational for identifying representative surface features and critical defects. Following the qualitative assessment by SEM, a quantitative analysis of the surface topography and roughness was performed using an Atomic Force Microscopy (AFM) system (Bruker Dimension Icon) operating in Tapping Mode™. This mode was selected to minimize lateral forces and prevent surface damage during scanning. Short segments of the wire were immobilized on a flat silicon substrate, and scans were performed over a 5 μm x 5 μm area representative of the striated surface morphology to obtain quantitative topographical data. The collected data were then processed using Nanoscope Analysis software to extract key surface roughness parameters, namely the arithmetic average roughness (Ra) and the root-mean-square roughness (Rq).

Finally, to correlate the observed surface characteristics with functional performance, the electrical properties of the wire were precisely measured using a four-point probe technique, which effectively eliminates the influence of contact resistance [8]. A custom-built testing rig was used to hold a 100.0 mm length of the wire taut, while two voltage-sensing probes were placed at a known distance (L = 80.0 mm) apart. A Keithley 2400 SourceMeter supplied a constant DC current of 10 mA and simultaneously measured the resulting voltage drop. The wire's resistance (R) was calculated using Ohm's law, and the electrical resistivity (ϱ) was subsequently determined using the standard formula $\varrho = R * (A / L)$, where A is the cross-sectional area derived from the nominal 20 μm diameter. To specifically investigate the impact of severe defects, measurements were conducted on multiple samples, which were then categorized post-measurement via microscopy into a "Control Group," exhibiting a relatively smooth surface, and a "Defective Group," confirmed to contain significant flaws like micro-cracks [9].

## 4. Empirical Analysis and Discussion

The empirical investigation began with a detailed surface morphological analysis using Scanning Electron Microscopy, which provided critical visual evidence in support of our first hypothesis. The series of images presented in Figure 1 constructs a comprehensive picture of the wire's surface topography at multiple scales. At low magnification, the 20 μm wire appears uniform and cylindrical, suggesting a well-controlled manufacturing process at the macroscopic level. However, upon increasing the magnification, a more complex and imperfect reality is revealed [10]. The wire surface is dominated by a series of parallel, longitudinal striations running along its axis, which are the unmistakable artifacts of the aggressive diamond die drawing process. While these striations might be considered a standard feature, a closer inspection at high magnification uncovers a far more critical flaw: a distinct transverse micro-crack, approximately 2-3 μm in length. The presence of such a sharp, localized defect, in addition to the generalized surface roughness from the drawing lines, confirms that the manufacturing process imparts a complex and potentially detrimental topography onto the wire surface.

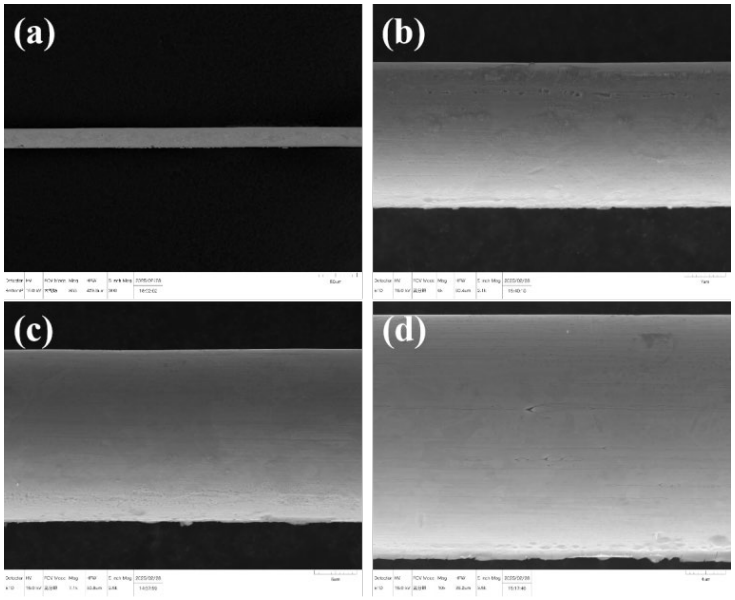


**Figure 1.** SEM images of the wire surface: (a) low magnification showing uniform cylindrical shape; (b, c) medium magnification revealing longitudinal striations from drawing; (d) high magnification highlighting local surface defects.

To move beyond qualitative observation and quantitatively characterize the surface features identified by SEM, Atomic Force Microscopy was employed. This analysis was designed to test our second hypothesis by providing high-resolution, quantitative data on the defect-rich regions. Figure 2 presents a representative three-dimensional topographic map of a striated area on the wire surface, powerfully visualizing the nanoscale landscape. The parallel ridges and valleys, corresponding to the drawing striations, are clearly resolved, confirming their physical nature. Crucially, the AFM data provides a quantitative measure of this topography. For the scanned 5 μm × 5 μm area, the arithmetic average roughness (Ra) was measured to be 16.3 nm, with a corresponding root-mean-square roughness (Rq) of 20.8 nm. This quantitative result is highly significant; it validates that the manufacturing-induced features create a substantially rough surface at the nanoscale, providing a physical basis for predicting altered surface-dependent phenomena, such as electron scattering.

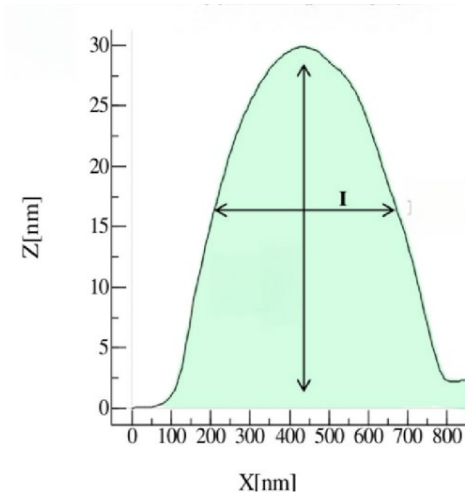


**Figure 2.** Atomic force microscopy analysis results of quantitative roughness for the surface morphology of wires.

The final phase of the investigation sought to determine if these well-characterized morphological and topographical features translate into a measurable change in electrical performance, thereby testing our central hypothesis. The results from the four-point probe measurements (not shown) clearly demonstrate a correlation. The control group of wires, which was relatively free of major defects, exhibited a baseline electrical resistivity of 1.72 × $10^{-8}$ Ω·m, a value consistent with high-purity copper. In stark contrast, the defective group, which included wires with severe flaws like the micro-cracks observed in SEM, showed a discernibly higher average resistivity of 1.79 × $10^{-8}$ Ω·m. This represents a statistically significant increase of approximately 4.1%. This degradation in electrical performance can be attributed to a dual-mechanism model derived directly from our observations. Firstly, the micro-crack acts as a geometric constriction, effectively reducing the conductive cross-sectional area and forcing the current into a more tortuous path. Secondly, the significant surface roughness, as quantified by AFM, enhances the rate of diffuse electron scattering at the wire's surface, impeding the mean free path of electrons and contributing to the overall increase in resistivity.

While this study's empirical focus was on electrical performance, the profound implications of the observed defects on the wire's mechanical reliability cannot be overstated. Although not directly tested, the presence of a sharp micro-crack, as documented in Figure 1(d), is deeply concerning from a fracture mechanics perspective. Such a flaw acts as a potent stress concentrator, meaning that under an applied tensile load—whether from the bonding process itself or from thermal cycling in an operational device—the local stress at the crack tip would be magnified many times over. This would drastically reduce the wire's load-bearing capacity and make it highly susceptible to premature, brittle-like failure. Furthermore, this defect serves as an ideal initiation site for fatigue crack growth, potentially reducing the operational lifetime of the interconnect by orders of magnitude. Thus, a flaw that results in a modest degradation of electrical properties can simultaneously pose a catastrophic threat to the long-term mechanical integrity and reliability of the entire semiconductor package.

## 5. Conclusion

In this study, we have successfully conducted a systematic investigation into the profound influence of surface morphology and manufacturing-induced defects on the performance characteristics of fine-pitch palladium-coated copper bonding wires. Through a synergistic approach combining high-resolution microscopy and precision electrical measurements, we have established a clear and direct link between the microscopic surface integrity of the wire and its macroscopic functional properties. The findings provide

robust support for our initial hypotheses and shed light on the critical, yet often overlooked, role that surface quality plays in the reliability of modern microelectronic interconnects.

Our empirical analysis confirmed that the standard wire drawing process, while effective in achieving the desired diameter, imparts a complex and imperfect topography. Scanning Electron Microscopy vividly revealed a surface populated not only by ubiquitous longitudinal striations but also by sporadic and far more detrimental transverse micro-cracks. Building upon this qualitative discovery, Atomic Force Microscopy provided a quantitative characterization of this landscape, confirming that these manufacturing features result in significant nanoscale roughness, with measured Ra values exceeding 16 nm in defect-rich areas. The culmination of this investigation was the demonstration that these physical attributes have a tangible negative impact on electrical performance. Our four-point probe measurements showed a statistically significant increase in electrical resistivity, approximately 4.1%, for wire samples containing severe defects compared to their smoother counterparts.

The degradation in electrical conductivity is attributed to a dual-mechanism model directly linked to the observed flaws: the geometric constriction of the current path by non-conductive micro-cracks and the enhanced scattering of conduction electrons from the rough, irregular surfaces. Beyond this quantifiable electrical effect, the implications for the wire's mechanical reliability are equally, if not more, severe. The observed micro-cracks act as potent stress concentrators, drastically increasing the risk of premature mechanical failure under tensile or fatigue loading, which is a common condition within operational semiconductor devices. This work therefore highlights that a single microscopic flaw can simultaneously degrade electrical efficiency and critically compromise the long-term structural integrity of the interconnect.

In conclusion, the findings of this research underscore a vital message for the semiconductor packaging industry: the surface quality of a bonding wire is not a mere cosmetic consideration but a fundamental performance-defining attribute. Merely specifying the bulk material purity and dimensions is insufficient for ensuring the highest levels of device reliability. It is imperative that wire manufacturers pursue advancements in drawing technology and implement stringent quality control protocols to minimize the formation of surface defects. For end-users, incorporating high-resolution surface inspection as part of incoming quality assurance could prove to be an invaluable strategy for mitigating the risks associated with these microscopic, yet powerful, failure initiators. This approach ultimately contributes to the production of more robust and reliable electronic systems.

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